Upgrade of the Distributed Time-Keeping and Synchronization System for EAST*

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Abstract The distributed time-keeping and synchronization system (DTSS) underwent an upgrade for EAST during the last shutdown. The upgraded DTSS, designed based on PXI bus and reconfigurable I/O devices, synchronizes all other sub-systems by using a reference clock and trigger. It can produce a uniform clock up to 80 MHz, provide a delayed trigger from 1 ms to 6872 s in 1 ms steps with 10 ns accuracy, and acquire the outputs of itself for self-inspection. The new DTSS was successfully applied in the 2012 spring EAST campaign, and has proven to be stable and reliable, giving an effective performance. The system structure and software development will be illustrated in detail in this paper.

Keywords: timing, synchronization, EAST, PXI, reconfigurable I/O

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1 Introduction

Significant progress has been made on EAST during the 2012 spring experimental campaign on many physical and technological aspects, such as the achievement of long pulse H-modes over 30 s with LHCD and ICRH facilitated by active lithium (Li) and cryopumping [1]. EAST consists of many subsystems such as a vacuum system, poloidal field (PF) power supply [2], plasma current drive and heating system, which are located in different places and need to be run by a synchronization control system to trigger them at specified times to maintain the fusion device operation stability.

A microcontroller and an field programmable gate array (FPGA) device were used in the former center timing (time-keeping) system (CTS) to provide 16 signal outputs with unification clocks (0.01 Hz~10 MHz) and different delay times (1~4294 s); the precision of the CTS is better than 1 ms [3,4], but the functions and the number of the output channels can not meet the requirement of the diagnostic systems with the development of real-time control in the EAST experiment.

The upgraded distributed timing and synchronization system (DTSS) is an expandable and real-time control system which has been developed for the EAST fusion experiment with three goals: (i) to provide the timing signals, ensuring each subsystem works in accord with the same reference clock; (ii) to provide the trigger signals, controlling the participation in the experiment of subsystems in proper time series; (iii) to acquire the outputs of itself, inspecting the operation state of DTSS automatically [5].

The new DTSS keeps the original star-type topology [6] with a central node and several local nodes. All the nodes are implemented in the PXI and FPGA industry devices. A PXI chassis with a controller, a timing I/O module and a multifunction RIO with FPGA device are used in a DTSS local node. The central and local nodes have similar configuration except that the former has two timing I/O modules, with an additional module used for producing the synchronized clock. The architecture of the new DTSS and the description of the DTSS’s units will be presented in the following sections.

2 System architecture

Based on the virtual instrument technique, the DTSS is designed in a distributed structure which is composed of a console host, a database server, the synchronized network, one central PXI node (CPN), several local PXI nodes (LPNs) and some isolation and drive modules. The structure of the DTSS with two LPNs is illustrated in detail in Fig. 1.

All the devices are linked by the synchronized net, namely EAST control net, the trigger synchronization net and the timing synchronization net [7]. Parameters for each node are set on the console host and transmitted to the PXI nodes and database server through the gigabit EAST control network. The trigger synchronization net is used to deliver the “Start/Stop” signal which is generated by the central control system (CCS) to drive all the PXI nodes to work/stop at the same time. The timing synchronization net is used to distribute the synchronization clock signals to LPNs for phase lock to the oscillator of the CPN. The lengths of

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all the fibers are equal, which ensures the signals transmitting from the CPN to all LPNs to have the same path length of fiber optic transmission \[4\]. All the outputs are transmitted to the subsystems after isolation and drive device. Six trigger outputs are acquired by analog input (AI) channels and these data are stored in the local disk in Lempel-Ziv-Oberhumer (LZO) format.

3 The description of the DTSS units

3.1 Console host

A human-machine interface program on the console host, developed with LabVIEW graphics language, is the interface software for the operators in the EAST main control room to configure and preset plasma discharge scenario before each experiment shot \[8\]. The physical channels can be indexed according to the number of nodes, the name of the subsystem or the discharge time sequence. Parameters such as delay time are modified by the operator and delivered to all of the PXI nodes through EAST control network. At the same time, these parameters are stored in the remote database server.

3.2 Database server

The database server based on Linux and Mysql supports multi-user and multi-thread access at the same time stably and efficiently \[8\]. A database named dtss-data is set up in the server, which includes a main table called dtss-data_db. This table includes pre-defined characteristics, such as channel_id, channel_name, delay, pulse, sig_polarity, etc. Channel_id is defined as the index of the table, to improve the speed of the data retrieval and renewal. The main field definition and function of dtss-data_db are summarized in Table 1.

3.3 Synchronized network

As mentioned above, the synchronized network consists of three parts. EAST control network is used to communicate and exchange messages among devices through TCP/IP socket. The synchronization clocks and system-start trigger signals are broadcast from the CPN to LPNs through the timing synchronization net and trigger synchronization net. The longest distance between the CPN to the LPN is 158 m, so all the fiber lengths are made at 158 m to guarantee that signals arrive at different nodes with the synchronized clock and the same delay \[9\]. The use of dual optical fibers removes ground loops among different systems, eliminates noise pick-up and provides high voltage isolation \[3\] among different systems.

<table>
<thead>
<tr>
<th>Field name</th>
<th>Type</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel_id</td>
<td>Int</td>
<td>The unique number to identify the physical channel</td>
</tr>
<tr>
<td>Channel_name</td>
<td>Varchar</td>
<td>Describes the main function of each channel</td>
</tr>
<tr>
<td>Delay</td>
<td>Int</td>
<td>Sets delay time for each trigger channel</td>
</tr>
<tr>
<td>Pulse</td>
<td>Int</td>
<td>Sets pulse width for each trigger</td>
</tr>
<tr>
<td>Sig_polarity</td>
<td>Enum</td>
<td>Sets the signal polarity, such as positive or negative</td>
</tr>
<tr>
<td>En_disable</td>
<td>Enum</td>
<td>Offers the option of enabling trigger</td>
</tr>
<tr>
<td>Shotno</td>
<td>Int</td>
<td>Describes the current shot number</td>
</tr>
</tbody>
</table>
3.4 Central PXI node

The CPN is implemented in a PXI-1042Q 8-slot chassis, which is equipped with a PXI-8110 controller running on LabVIEW Real-Time system, two PXI-6608 timing I/O modules, and a PXI-7842R multifunction RIO device. The first timing module generates a 5 V square wave synchronization clock at 10 MHz to the backplane of each PXI node, ensuring all the nodes work on the same time-base. The second timing I/O module offers the subsystems with high-precision reference clocks that frequency can be set by operator. The FPGA in RIO device is customized to realize pulse generator and acquisition, etc. The block diagram of CPN is presented in Fig. 3.

![Fig.3 Block diagram of the CPN (color online)](image)

The main logic is encapsulated in various application modules and all the application modules in the diagram are named after their functions. The acquisition module, for example, acquires the external event or the outputs of itself at the sampling rate of 100 KHz.

Different from DIII-D and JET, data are mostly served in LZO format in the EAST distributed data system. EASTScope which is supplied by the computer application division of ASIPP is a special data analysis and visualization software for the LZO file. The data compress module’s function is to compress the digitized data into LZO files. The program diagram of the data compress module (DCM) is illustrated in Fig. 4.

![Fig.4 Program diagram of DCM (color online)](image)

The LZO compress algorithm dynamic link library (DLL) has been written in the C++ programming language. The call library function node (CLFN), which is used to create an interface to the external code, calls the DLL directly. The input parameters are wired to the left terminal of the CLFN in the same order as they appear in the DLL function declaration. An array of oriData is comprised of floating point numbers with single (4-byte) precision which is transferred by the acquisition module, so the data buffer for the LZO DLL is 4 times of the oriData array dimension. The trigTime, devName, sigName, etc. are all input parameters in the LZO algorithm for the LZO DLL. The output of the CLFN at the right terminal stands for the data compression state of DCM. The value of lzoflag equals to 0 means that DCM completes the data compression successfully. The method offered here can be extended to other development of DLL files.

3.5 Local PXI node

Relying on the synchronization clock signals, the LPN can be phase-locked to the oscillator of the CPN. All the modules in the LPN play the same role as the modules in the CPN except that the LPN contains only one clock module for distributing high-stability reference clocks to subsystems. 8 high-precision counters in PXI-6608 generate 8 reference clock signals. The FPGA in PXI-7842R provides a subsystem with 90 channels for a single trigger. Six analog input channels in PXI-7842R realize the function of acquisition for self-inspection.

In order to fulfill the requirements of some diagnostic systems, a single channel multi-trigger module is implemented during the experimental campaign. The configuration of hardware and the block diagram of LPN have similar structures as the CPN. It offers subsystems with 10 trigger channels, and each channel generates as many as a 4 triggers sequence. The parameter setting GUI for this module is published as a web page to facilitate the users. All the parameters in Fig. 5 should be pre-defined before a new shot and the OK button ensuring the setting. On discharging, the current shot number will update as well as the experiment status, and the OK button is prevented from working, to warn the users that they are unable to make any changes.

3.6 Isolation and drive module

The isolation and drive module is designed to remove ground loops among different systems, and each output channel on the PXI node has an independent power supply [8]. VHDCI (very-high-density cable interconnect) connector shielded cable is used to connect the PXI card with this device, so the TTL signals generated from the PXI RIO module can be changed into the optical signal and transmitted to the diagnostic system through the optic network directly. With an electric-optic (E/O) conversion circuits, Agilent HFBR-1414T is chosen to drive reference clock optic signals for the subsystems, and the clock signals transmitted through the fiber optical network are converted by an HFBR-2412 optic-electric (O/E) receiver circuit [4]. A new isolation and drive module will be customized in the future with higher bandwidth.
4 Test results

Under the star-type topology, the synchronization of trigger output is one of the most critical indexes for the DTSS. Two trigger signals are respectively acquired from two different LPNs. These trigger channels have the same delay parameters: delay time: 0, pulse width: 10 ms, sig_polarity: positive, en/disable: enable. Fig. 6 shows the results by using the Tektronix™ MSO4034 mixed signal oscilloscope. In Fig. 6(a), the timescale is set to 2.00 ms/div and the sampling rate is 500 MS/s. The pulse-widths of the two signals are 10 ms, which equals the pulse-widths of the preset pulses. In Fig. 6(b), the timescale is set to 20 ns/div and the sampling rate is 2.5 GS/s. The rising edges between the two positive signals are less than 10 ns. So the trigger signals with the same preset parameters in two different LPNs have good time synchronization and the maximum time difference is less than 10 ns.

In order to inspect the correctness of triggers, the trigger outputs are acquired by DTSS at the sampling rate of 100 K/s. Those signals which were compressed into LZO files will be viewed by EASTScope. The CH 9 (channel 9) of the single channel multi-trigger, which is generated by the 2nd LPN located in the machine hall, is shown in Fig. 7.

The CH 9 parameters for shot 38608 in Fig. 5 are listed below. The CH 9 output enables 4 triggers. 1st delay time: −5000 ms, pulse width: 500 ms; 2nd delay time: −4000 ms, pulse width: 500 ms; 3rd delay time: −3000 ms, pulse width: 500 ms; 4th delay time: −2000 ms, pulse width: 500 ms. The sig_polarity is positive. Fig. 7 shows that they are 4 positive delay triggers in CH 9, and the start times of the sequence are around −5000 ms, −4000 ms, −3000 ms and −2000 ms. Their pulse-widths are all about 500 ms. The result is consistent with the pre-set parameter above.

Fig. 6 Test result of two LPNs’ delayed triggers. (a) timescale is set to 2.00 ms/div, sampling rate is 500 MS/s, (b) timescale is set to 20 ns/div, sampling rate is 2.5 GS/s (color online)

The channels test results in laboratory, as shown in Fig. 6, demonstrate its accuracy, and the system has been successfully applied to the EAST campaign since 2011, which also confirms the reliability of the system logic. Although only six channels are acquired and the sampling precision is low, it is a satisfactory solution for trouble-shooting when the user receives trigger-fail messages from the subsystem.
5 Conclusions

The new DTSS can provide a reference clock in frequency up to 80 MHz, produce delayed trigger signals from 1 ms width to about 6872 s maximum duration with 10 ns accuracy, and the multi-trigger module in LPN generates as many as 4 triggers sequence in one channel. The ability to acquire signal input/output is also integrated into this system. The hardware, networks, database and LabVIEW software use standard commercial components, which provide an open and flexible architecture that can be easily modified [7], and the modular design is also conductive to expand the system functions for future improvement.

The new DTSS was successfully applied in the 2012 spring EAST campaign, and has proven to be stable and reliable, giving an effective performance. To convert high-speed clock signals, a new isolation and drive module will be customized in the future with higher bandwidth.

References

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